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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,363	10/31/2003	Shin-Hung Yeh	250122-1050	3014

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THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
100 GALLERIA PARKWAY, NW
STE 1750
ATLANTA, GA 30339-5948

EXAMINER	
PERVAN, MICHAEL	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,363	YEH, SHIN-HUNG	
	Examiner	Art Unit	
	Michael Pervan	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 7* is/are rejected.

7)☒ Claim(s) *2-6 and 8-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsueda (US 6,873,312) in view of Maekawa (US 6,256,024).

In regards to claim 1, Matsueda discloses (Figures 1, 7 and 11) a digital data driver (2), comprising: a plurality of data lines (17), each transferring first data (data on line D1 at the time of transfer) during a first period (SR1) and second data (data on the line D2 at the time of transfer) during a second period (SR2); a first shift register outputting a first enable signal (SR1) during the first period; a second shift register outputting a second enable signal (SR2) during the second period; and a plurality of transmission controllers (12, 13, 14) coupled to the plurality of data lines respectively, each having first to fourth latches (top right latch is 1, top left is 2, bottom right latch is 3 and bottom left latch is 4); wherein each transmission controller stores the first data and the second data in the second latch and the first latch respectively according to the first enable signal and the second enable signal (col. 8, lines 10-22; first data (D1) goes into latch 2 on SR1 and second data D2 goes into latch 1 on SR2); each transmission controller outputs the first data stored in the second latch to the fourth latch and outputs to a DAC according to a third enable signal (col. 8, lines 23-32; when the LP (3rd and 4th

enable signal) occurs the data in latch 2 goes to latch 4 and then to the DAC); each transmission controller outputting the second data stored in the first latch to the third latch (col. 8, lines 23-32; when the LP (3rd and 4th enable signal) occurs the data in latch 1 goes to latch 3) and outputs to a second DAC according to a fourth enable signal (col. 8, lines 23-32; when the LP (3rd and 4th enable signal) occurs the data in latch 2 goes to latch 4 and then to the DAC).

Matsueda does not disclose a first inverter and outputting to a second DAC through the first inverter.

Maekawa discloses (Figures 1, 2 and 4) a first inverter (36) and outputting to a second DAC through the first inverter (col. 3, lines 27-33; by the data going through the latch it also goes through the first inverter and is inputted into the DAC).

It would have been obvious at the time of invention to modify Matsueda by incorporating the teachings of Maekawa, data output from a latch (16) through an inverter (36) and input to a DAC (17), by replacing the 3rd latch of Matsueda with the latch of Maekawa because the inverter being part of latch (16) enables the circuit to output rapidly amplified signal having a signal level required to process subsequent circuits (col. 4, lines 57-63).

In regards to claim 7, Matsueda discloses (Figures 1, 7 and 11) a liquid crystal display (1), comprising: a plurality of pixels arranged in a matrix (6); a scan driver (3) turning on each row of pixels arranged in the matrix sequentially; and a digital data driver (2) outputting data to the corresponding pixels, each comprising: a plurality of data lines (17), each transferring first data (data on line D1 at the time of transfer) during

a first period (SR1) and second data (data on the line D2 at the time of transfer) during a second period (SR2); a first shift register outputting a first enable signal (SR1) during the first period; a second shift register outputting a second enable signal (SR2) during the second period; and a plurality of transmission controllers (12, 13, 14) coupled to the a plurality of data lines respectively, each having first to fourth latches (top right latch is 1, top left is 2, bottom right latch is 3 and bottom left latch is 4); wherein each transmission controller stores the first data and the second data in the second latch and the first latch respectively according to the first enable signal and the second enable signal (col. 8, lines 10-22; first data (D1) goes into latch 2 on SR1 and second data D2 goes into latch 1 on SR2); each transmission controller outputs the first data stored in the second latch to the fourth latch and outputs to a DAC according to a third enable signal (col. 8, lines 23-32; when the LP (3^{rd} and 4^{th} enable signal) occurs the data in latch 2 goes to latch 4 and then to the DAC); each transmission controller outputting the second data stored in the first latch to the third latch (col. 8, lines 23-32; when the LP (3^{rd} and 4^{th} enable signal) occurs the data in latch 1 goes to latch 3) and outputs to a second DAC according to a fourth enable signal (col. 8, lines 23-32; when the LP (3^{rd} and 4^{th} enable signal) occurs the data in latch 2 goes to latch 4 and then to the DAC).

Matsueda does not disclose a first inverter and outputting to a second DAC through the first inverter.

Maekawa discloses (Figures 1, 2 and 4) a first inverter (36) and outputting to a second DAC through the first inverter (col. 3, lines 27-33; by the data going through the latch it also goes through the first inverter and is inputted into the DAC).

It would have been obvious at the time of invention to modify Matsueda by incorporating the teachings of Maekawa, data output from a latch (16) through an inverter (36) and input to a DAC (17), by replacing the 3rd latch of Matsueda with the latch of Maekawa because the inverter being part of latch (16) enables the circuit to output rapidly amplified signal having a signal level required to process subsequent circuits (col. 4, lines 57-63).

Allowable Subject Matter

3. Claims 2-6 and 8-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art (Tanaka US 6,356,223) is deemed relevant since it discusses four latches, two shift registers and DACs. The prior art (Koyama et al US 6,693,616) is deemed relevant since it discusses multiple latches, shift registers and DACs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Pervan whose telephone number is (571) 272-0910. The examiner can normally be reached on Monday - Friday between 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MVP
Apr. 26, 2006

AMR A. AWAD
PRIMARY EXAMINER